REMARKS

Claims 13-25 are pending. Claim 25 has been added. Claims 13-19, 23 and 24 have been amended. No new matter has been introduced. Reexamination and reconsideration of the present application is respectfully requested.

Applicant has enclosed herewith an Information Disclosure Statement ("IDS") and a copy of the reference cited therein. Applicant respectfully requests that the Examiner enter the IDS and consider the reference.

In the July 17 Office Action, the Examiner objected to claim 17 for informalities. Applicant has amended claim 17 in view of the Examiner's comments. Accordingly, Applicant respectfully submits that the objection should be withdrawn.

The Examiner indicated that claims 16 and 23 would be objected to under 37 C.F.R. 1.75 as being substantially duplicative of claims 15 and 22, if claims 15 and 22 were found allowable. Applicant has amended claims 16 and 23 in view of the Examiner's comments. Accordingly, Applicant respectfully submits that the objection should be withdrawn.

The Examiner indicated that claim 19 would be objected to under 37 C.F.R. 1.75 as being substantially duplicative of claims 14, if claim 14 were found allowable. The Examiner also indicated that claim 18 would be objected to under 37 C.F.R. 1.75 as being substantially duplicative of claims 13, if claim 13 were found allowable. Applicant respectfully submits that claims 14 and 19 are not substantially duplicative and differ in scope because claim 14, as amended includes limitations which are not present in claim 19, as amended, and vice versa. Specifically, claim 14, as amended requires a "plurality of compressed image data, each of which is comprised of a plurality of blocks having a predetermined size" and "a first storage device which serves as a first-in-first-out memory." Claim 19 does not include either of these

limitations. On the other hand claim 19, as amended specifies "the display device does not start making a read access to the second storage device until the writing device starts making a write access to the first storage device, and the display device starts making the read access to the second storage device when the writing device starts making the write access to the first storage device.". However, independent claim 14, as amended is not so limited. Accordingly, Applicant respectfully submits that the objection with respect to independent claims 14 and 19 should be withdrawn.

Similarly, with respect to claims 13 and 18, Applicant respectfully submits that claims 13 and 18, as amended, differ in scope. In particular, claim 13, as amended requires "a first reading device for making a read access to a memory that stores a plurality of compressed image data, each of which are is comprised of a plurality of blocks each having a predetermined size in advance, so as to read the compressed image data block-by-block" and "a first storage device serving as a first-in-first-out memory". Independent claim 18, as amended does not include either of these limitations. On the other hand, independent claim 18, as amended specifies that "the display device does not start making a read access to the second storage device until the writing device starts making a write access to the first storage device, and the display device starts making the read access to the second storage device when the writing device starts making the write access to the first storage device." However, independent claim 13, as amended is not so limited. Accordingly, Applicant respectfully submits that the objection with respect to independent claims 13 and 18 should be withdrawn.

The Examiner rejected claims 13-24 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement and failing to satisfy the enablement requirement. In doing so, the Examiner states that the claims contain subject matter which was

not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully disagrees. With reference to claims 13-24, Applicant notes that the claimed second storage device corresponds to the frame buffer and that sprite pattern, which is produced by the decoder, is written into the sprite buffer. Further, the write operation into the sprite buffer is described in the specification as expansion access (or expand), while the claims use the term writing (or write).

In addition, Applicant notes that the feature in which a priority is given in the write operation of the sprite buffer rather than the read operation is supported by pages 10 and 11 of the specification as filed. In particular, the specification states:

> In order to draw an image by writing data into the frame buffer 23, it is necessary to read sprite pattern data from the sprite buffer 18. The sprite buffer interface 17 gives a first priority in making an access for expansion of sprite pattern data in the sprite buffer 18 in order not to break the decoding process in progress in the decoder 16. Therefore, the sprite buffer interface 17 performs reading operations for reading sprite pattern data from the sprite buffer 18 in a prescribed time period in which it does not proceed an access for expansion of sprite pattern data. This indicates that during such expansion access period for expansion of sprite pattern data, it is impossible for the image processing device 11 to draw an image in association with the frame buffer. (Page 10, line 24 – page 11, line 8)

Further the technical feature in which a priority is given in the read operation of the frame buffer rather than the write operation is supported by the description on page 11 of the specification as filed. Specifically, the specification states:

> The frame buffer interface 22 gives a first priority in making an access for displaying an image stored in the frame buffer 23 (i.e., an access for reading data

from the frame buffer 23) in order to prevent noise from occurring on the screen of the display 4. This indicates that during such a display access period for display an image stored in the frame buffer 23, it is impossible for the image processing device 11 to draw an image in association with the frame buffer 23. Accordingly, Applicant respectfully submits that the rejection should be withdrawn.

The Examiner rejected claims 13-24 under 35 U.S.C. 103 (a) as being unpatentable over Ito, JP2002-341859 (hereinafter Ito) in view of Xie, U.S. Patent Application Publication No. 2005/0024369 A1 (hereinafter Xie), Snyder et al., U.S. Patent No. 6,326,964 (hereinafter Snyder) and Witzig et al., C. Witzig, S. Adler, E787 Technical Note #264, 1993 (hereinafter Witzig). Applicant respectfully traverses the rejections in view of the claims as amended.

Independent claim 13, as amended now recites:

An image processing device comprising:

a first reading device for making a read access to a memory that stores a plurality of compressed image data, each of which is comprised of a plurality of blocks each having a predetermined size in advance, so as to read the compressed image data block-by-block;

a decoder for decoding the compressed image data block-by-block so as to produce decompressed image data;

a ***first storage device serving as a first-in-first-out memory, which is given a priority in a write operation for writing the decompressed image data therein rather than a read operation for reading the decompressed image data therefrom***, and is incapable of simultaneously performing the write operation and the read operation and has a storage area operable for storing a plurality of decompressed image data decoded by the decoder;

a writing device for writing the decompressed image data into the first storage device block-by-block;

a second reading device for reading the decompressed image data from the first storage device;

a second storage device that is given a priority in a read operation for reading therefrom rather than a write operation for writing therein and is incapable of simultaneously performing the read operation and the write operation;

a control device for performing prescribed processing on the image data read from the first storage device and for writing the processed image data into the second storage device; and

a display device for reading the processed image data from the second storage device and for displaying an image based on the processed image data.

The present invention is directed to an improved image processing device. In the conventionally-known image processing device, an expansion process for expanding one sprite pattern into the sprite buffer is performed in synchronization with a drawing process for drawing and rendering one sprite pattern into the frame buffer. This raises a problem in that, when the rendering and drawing in the frame buffer takes a relatively long time, it is impossible to perform an expansion process for expanding the next sprite pattern before the completion of the rendering and drawing; and this reduces the drawing performance of the image processing device.

In order to solve the aforementioned problem, the image processing device recited in independent claim 13, as amended includes a first storage device (e.g., a sprite buffer), which has a storage area capable of storing a plurality of expanded image data and which serves as a FIFO memory and in which the write operation is given a priority rather than the read operation because the read operation and the write operation cannot be performed simultaneously, and a second storage device (e.g., a frame buffer) in which the read operation is given a priority rather than the write operation because the write operation and read operation cannot be performed simultaneously, wherein one compressed image data representing, for example a sprite pattern, each having a prescribed size are read from the memory block-by-block and are decoded to produce expanded image data, which are then written into the first storage device block-by-block, and wherein the image data read from the first storage device are subjected to prescribed processing and are then stored in the second storage device, so that the processed image data area read from the second storage device and are then displayed.

Since the first storage device serves as a FIFO memory having a storage area capable of storing a plurality of expanded image data, and the compressed image data are formed in a plurality of blocks so that the decoding, read operation, and write operation are performed block-

by-block, it is possible to perform the write operation (or expansion process) for writing one compressed image data representing, for example a sprite pattern into the first storage device (e.g., a sprite buffer) and the drawing process for performing prescribed processing (i.e., rendering) of one compressed image data (e.g. sprite pattern) and for drawing it into the second storage device (e.g., a frame buffer) in an asynchronous manner. Thus, even though the rendering and drawing of the compressed image data in the second storage device takes a relatively long time, it is possible to start the expansion process of the next compressed image data (e.g., the next sprite pattern) block-by-block in the first storage device before the completion of the rendering and drawing. The first storage device is configured such that the write operation is given a priority rather than the read operation, whereby it is possible to efficiently implement the expansion process of the compressed image data irrespective of the drawing in the second storage device.

Irrespective of the performance of the second storage device in which the read operation is given a priority rather than the write operation (or drawing), the compressed image data constituted by a plurality of blocks are subjected to decoding, read operation, and write operation block-by-.block. Compared with the conventionally-known technology in which one compressed image data, which are not constituted by a plurality of blocks, are collectively subjected to drawing into the frame buffer, it is possible for the present invention to increase the chance for making drawing accesses to the second storage device, thus improving the drawing performance of the image processing device.

Further, since the decoder is configured to perform decoding block-by-block, the size of the buffer of the decoder for storing the decoding results can be reduced.

The Ito reference does not disclose, teach, or suggest the device specified in independent

claim 13. Unlike the device specified in claim 13, Ito does not teach a device which includes "a ***first storage device serving as a first-in-first-out memory, which is given a priority in a write operation for writing the decompressed image data therein rather than a read operation for reading the decompressed image data therefrom.***"

Ito teaches an image processing device with a sprite buffer and a frame buffer. Ito discloses that pattern data which belongs to the most subordinate sprite in priority read out first from the sprite attribution table, are decompressed and converted to RGB data. The rendering process is then made on them and they are written into the frame buffer 39. Thereafter, attribution data of a second sprite are read out from the sprite attribution table 23, and sprite pattern data of the second sprite are read out from pattern ROM 25 based upon the sprite attribution data. The data being read out are decompressed and converted to RGB data, then the rending process is made on them and they are written into the frame buffer 39. This process is then repeated until all of the sprites that are predetermined are written into the frame buffer 39. At this point, the RGB data stored into the frame buffer 40 are read out in order and outputted to the display device 26. *(Ito; page 10, paragraph 0017- page11, paragraph 0018)*

In other words, as the Examiner has acknowledged, Ito discloses that a read operation is given priority over a write operation. In particular, the Examiner states that "the Ito reference clearly teaches that it is optimal to have a sprite buffer because it increases the data throughput [0021-0023], and that the **read should get priority** [0017-0018], where this is suggested because of the fact that data must be read from the sprite buffer to the frame buffer to be written to the display, where it would be obvious that such data that any reads from data in the sprite buffer are going to be faster than write commands from the pattern ROM, which constitute write operation to the sprite buffer, because any request for data from the pattern ROM must be decoded and then

passed to the sprite buffer, meaning that it will always maximize data transfer to pull data from the sprite buffer first because it takes less time for that data to be written to the frame buffer [0022]." *(See July 17 Office Action, page 8 emphasis added)* However, the Ito reference does not disclose "*a first storage device serving as a first-in-first-out memory, which* ***is given a priority in a write operation for writing the decompressed image data therein rather than a read operation for reading the decompressed image data therefrom***."

In addition, the Ito reference fails to disclose, teach or suggest, ***"a second storage device that is given a priority in a read operation for reading therefrom rather than a write operation for writing therein and is incapable of simultaneously performing the read operation and the write operation"*** or ***"a first reading device for making a read access to a memory that stores a plurality of compressed image data, each of which is comprised of a plurality of blocks each having a predetermined size in advance, so as to read the compressed image data block-by-block."*** Accordingly, Applicant respectfully submits that independent claim 13 distinguishes over Ito.

The Xie reference does not make up for the deficiencies of Ito. Xie is directed to a system for processing and displaying video and graphics. *(Xie; page 1, paragraph 0003)* Xie discloses a display engine 2514 wherein the display engine 2514 has four graphic conversation pipelines for processing four overlapping graphics windows, and wherein each of the graphics pipelines has a graphics FIFO. *(Xie; FIG. 69 and page 60, paragraph 0769)* However, the combination of Ito and Xie does not disclose, teach, or suggest "*a first storage device serving as a first-in-first-out memory, which* ***is given a priority in a write operation for writing the decompressed image data therein rather than a read operation for reading the decompressed image data therefrom***" or ***"a second storage device that is given a priority in a read operation***

for reading therefrom rather than a write operation for writing therein and is incapable of simultaneously performing the read operation and the write operation." Accordingly, Applicant respectfully submits that independent claim 13, as amended distinguishes over Ito in combination with Xie.

The Snyder reference does not make up for the deficiencies of Ito and Xie. The Examiner utilizes Snyder to show storing data in block format. *(July 17 Office Action, page 11)* Snyder is directed a pre-processing method which prepares 3D objects for rendering to image layers in a layered graphics rendering pipeline. *(Snyder; Abstract)* Snyder discloses that texture data are processed in a cache in 8x8 samples of blocks. *(Snyder; Col. 21, line 9-Col. 22, line 15)* However, Snyder fails to suggest that the texture data is compressed and necessarily subjected to decoding. Thus, the combination of Ito, Xie, and Snyder does not disclose, teach, or suggest "*a first storage device serving as a first-in-first-out memory, which* ***is given a priority in a write operation for writing the decompressed image data therein rather than a read operation for reading the decompressed image data therefrom***" or ***"a second storage device that is given a priority in a read operation for reading therefrom rather than a write operation for writing therein and is incapable of simultaneously performing the read operation and the write operation."*** Accordingly, Applicant respectfully submits that independent claim 13, as amended distinguishes over Ito in combination with Xie and Snyder.

The Witzig reference does not make up for the deficiencies of Ito, Xie, and Snyder. Witzig discloses a first in first out (FIFO) buffer system. *(Witzig; page 1)* Witzig teaches that the FIFO system is applied to the event manager of the UNIX base. However, the combination of Ito, Xie, Snyder and Witzig does not disclose, teach, or suggest "*a first storage device serving as a first-in-first-out memory, which* ***is given a priority in a write operation for writing the***

decompressed image data therein rather than a read operation for reading the decompressed image data therefrom" or ***"a second storage device that is given a priority in a read operation for reading therefrom rather than a write operation for writing therein and is incapable of simultaneously performing the read operation and the write operation."*** Accordingly, Applicant respectfully submits that independent claim 13, as amended distinguishes over Ito in combination with Xie, Snyder, and Witzig.

Independent claims 13, 14, 17-19, and 24 recite limitation similar to those in independent claim 13, as amended. Accordingly, Applicant respectfully submits that claims 13, 14, 17-19, and 24 distinguish over Ito in combination with Xie, Snyder, and Witzig for reason similar to those set forth above with respect to claim 13.

Applicant respectfully submits that independent claims 18, 19, and 24 further distinguish over the combination of Ito, Xie, Snyder, and Witzig. In particular, the combination of Ito, Xie, Snyder, and Witzig also fails to disclose, teach, or suggest a display device wherein "***the display device does not start making a read access to the second storage device until the writing device starts making a write access to the first storage device, and the display device starts making the read access to the second storage device when the writing device starts making the write access to the first storage device.***"

Applicant notes that in the conventionally-known image processing device having both a sprite buffer and frame buffer, it is impossible to draw into the frame buffer during an expansion access to the sprite buffer and during a display access by way of the frame buffer. As such, the drawing performance of conventionally-known image processing device is reduced.

The image processing device recited in each of independent claims 18, 19, and 24 solves this problem because the display device, which reads the processed image data from the second

storage device and displays the processed image data, does not make a read access to the second storage device until the writing device makes a write access to the first storage device. When the writing device makes a write access to the first storage device, a read access is made to the second storage device. Thus, the dead time for writing to the first storage device and/or reading from the second storage device is reduced. Accordingly, Applicant respectfully submits that claims 18, 19, and 24 further distinguish over the combination of Ito, Xie, Snyder, and Witzig.

Claims 15 depends from independent claim 13. Claims 16 depends from independent claim 14. Claims 20 and 22 depend from claim 18. Claims 21, 23, and 25 depend from independent claim 19. Accordingly, Applicant respectfully submits that claims 15, 16, 20-23 and 25 distinguish over Ito in combination with Xie, Snyder, and Witzig for the same reasons set forth above with respect to claims 13, 14, 18 and 19.

///

///

///

///

///

///

///

///

///

///

///

///

Applicant believes that the claims are in condition for allowance. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference call would advance prosecution of the application.

Respectfully submitted,

PILLSBURY WINTHROP SHAW PITTMAN LLP

Date: December 14, 2006

By: _____
Roger R. Wise
Registration No. 31,204
Customer No. 24796

725 South Figueroa Street, Suite 2800
Los Angeles, CA 90017-5406
Telephone: (213) 488-7100
Facsimile: (213) 629-1033